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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,747	12/02/2003	Uday R. Savagaonkar	5038-312	6815

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,747	SAVAGAONKAR ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities: in the last line after "measuring", change the semicolon to a period. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hembree et al (6218848).

Regarding claim 1, Hembree et al disclose [see Fig. 3] a test method, comprising: setting an overdrive [via test system 16]; measuring [via resistivity measuring circuit 38] a contact resistance of at least one channel (electrical paths 34) in each of a plurality of dies (dice 12) on a wafer (wafer 10); computing [via tester 26] a per channel standard deviation responsive to measuring the contact resistance [via resistivity measuring circuit 38]; comparing [tester 26] the standard deviation on the at least one channel to a threshold; and increasing [tester 26] the overdrive responsive to comparing the standard deviation.

Regarding claim 2, Hembree et al disclose measuring the contact resistance [via resistivity measuring circuit 38] on the at least one channel (electrical path 34) comprises: forcing [via tester 26] a current through the at least one channel (electrical path 34);

measuring [via test circuitry 33] a voltage on the at least one channel (electrical path 34); and calculating [via test circuitry 33] the contact resistance responsive to the forcing and measuring.

Regarding claim 3, Hembree et al disclose measuring [via resistivity measuring circuit 38] the contact resistance comprises measuring [via resistivity measuring circuit 38] the contact resistance on channels on each of the plurality of dies (die 12).

Regarding claim 4, Hembree et al disclose measuring [via resistivity measuring circuit 38] the contact resistance comprises measuring [via resistivity measuring circuit 38] contact resistance on a group of channels (electrical paths 34) on each of the plurality of dies (12).

Regarding claim 5, Hembree et al disclose measuring [via resistivity measuring circuit 38] the contact resistance comprises measuring [via resistivity measuring circuit 38] the contact resistance of all of the dies (12) on the wafer (10).

Regarding claim 6, Hembree et al disclose measuring [via resistivity measuring circuit 38] the contact resistance comprises measuring [via resistivity measuring circuit 38] the contact resistance of a group of dies (12) on the wafer (10).

Regarding claim 7, Hembree et al disclose establishing a bare contact (contacts 22) with the at least one channel on each of the plurality of dies (12) prior to setting the overdrive.

Regarding claim 8, Hembree et al disclose comparing [via test circuitry 33] the overdrive to an overdrive limit prior to measuring [via resistivity measuring circuit 38] the contact resistance.

Regarding claim 9, Hembree et al disclose increasing [via tester 26] the overdrive if the standard deviation on the at least one channel (electrical path) of each of the plurality of dies (12) is less than the threshold.

Regarding claim 10, Hembree et al disclose repeating measuring [via resistivity measuring circuit 38] the contact resistance and computing [via tester 26] the standard deviation responsive to comparing the standard deviation.

Regarding claim 11, Hembree et al disclose [see Fig. 3] a test apparatus, comprising: means [test system 16] for setting an overdrive; means [via resistivity measuring circuit 38] for measuring a contact resistance on each of a plurality of dies (12) in a wafer (wafer 10); means [via tester 26] for computing a standard deviation for each contact resistance measured responsive to the means [via resistivity measuring circuit 38] for measuring the contact resistance; and means [via tester 26] for increasing the overdrive responsive to the means [via tester 26] for computing the standard deviation.

Regarding claim 12, Hembree et al disclose means [via resistivity measuring circuit 38] for measuring the contact resistance includes means [via resistivity measuring circuit 38] for measuring a contact resistance on at least one channel (electrical path 34) in each of the plurality of dies (12).

Regarding claim 13, Hembree et al disclose means [probe card 20] for establishing a bare contact (contacts 22) with each of the plurality of dies (12) on the wafer (10).

Regarding claim 14, Hembree et al disclose means [via test circuitry 33] for comparing the overdrive to an overdrive limit prior to measuring [via resistivity measuring circuit 38] the contact resistance.

Regarding claim 15, Hembree et al a disclose means [via tester 26] for increasing the overdrive increases the overdrive if the standard deviation is less than a predetermined threshold.

Regarding claim 16, Hembree et al disclose [see Fig. 3] a wafer test system (test system 16), comprising: a tester (tester 26) capable of generating wafer test signals; a wafer (wafer 10) including a plurality of dies (dice 12), each die (12) having a plurality of channels; a probe head (probe card 20) including a plurality of pins (contacts 22) capable of probing the plurality of channels on each of the plurality of dies (12) on the wafer (10); and a chuck (chuck 24) capable of placing the wafer (10) in contact with the probe head (20); where the tester (26) is capable of: communicating an overdrive to the chuck (24), the chuck (24) moving the wafer (10) towards the probe head (20) responsive to the overdrive; measuring [via resistivity measuring circuit 38] a contact resistance of at least one channel in each of the dies (12) of the wafer (10) using the probe head (20); computing [via test circuitry 33] a per channel standard deviation responsive to measuring the contact resistance, comparing [via test circuitry 33] the standard deviation on the at least one channel to a threshold; and increasing the overdrive responsive to the comparison.

Regarding claim 17, Hembree et al disclose the tester (26) is capable of measuring the contact resistance by: forcing a current through the at least one channel (electrical

path 34); measuring a voltage on the at least one channel (34); and calculating the contact resistance [via resistivity measuring circuit 38] responsive to the forcing and measuring.

Regarding claim18, Hembree et al disclose the tester (26) is capable of measuring the contact resistance by measuring [via resistivity measuring circuit 38] the contact resistance on all channels on each of the plurality of dies (12).

Regarding claim 19, Hembree et al disclose the tester (26) is capable of measuring the contact resistance by measuring [via resistivity measuring circuit 38] the contact resistance on a group of channels on each of the plurality of dies (12).

Regarding claim 20, Hembree et al disclose the probe head (20) is capable of establishing a bare contact (22) with all channels on each of the plurality of dies (12) on the wafer (10) prior to the tester (26) setting the overdrive.

Regarding claim 21, Hembree et al disclose the tester (26) is capable of comparing the overdrive to a limit prior to measuring the contact resistance.

Regarding claim 22, Hembree et al disclose the tester (26) is capable of increasing the overdrive if the standard deviation on all channels is less than the threshold.

Regarding claim 23, Hembree et al disclose the tester (26) is capable of repeating measuring the contact resistance and computing the standard deviation responsive to comparing the standard deviation.

Regarding claim 24, Hembree et al disclose [see Fig. 3] an article (test system 16) comprising a storage medium (tester 26) having stored thereon instructions, that, when executed by at least one device, result in: setting an overdrive [via test system 16]; measuring [via resistivity measuring circuit 38] a contact resistance of at least one channel (electrical paths 34) in each of a plurality of dies (dice 12) on a wafer (wafer 10);

computing [via tester 26] a per channel standard deviation responsive to measuring the contact resistance [via resistivity measuring circuit 38]; comparing [tester 26] the standard deviation on the at least one channel to a threshold; and increasing [tester 26] the overdrive responsive to comparing the standard deviation.

Regarding claim 25, Hembree et al disclose measuring the contact resistance [via resistivity measuring circuit 38] on the at least one channel (electrical path 34) comprises: forcing [via tester 26] a current through the at least one channel (electrical path 34); measuring [via test circuitry 33] a voltage on the at least one channel (electrical path 34); and calculating [via test circuitry 33] the contact resistance responsive to the forcing and measuring.

Regarding claim 26, Hembree et al disclose establishing a bare contact (contacts 22) with the at least one channel on each of the plurality of dies (12) prior to setting the overdrive.

Regarding claim 27, Hembree et al disclose comparing [via test circuitry 33] the overdrive to an overdrive limit prior to measuring [via resistivity measuring circuit 38] the contact resistance.

Regarding claim 28, Hembree et al disclose increasing [via tester 26] the overdrive if the standard deviation on the at least one channel (electrical path) of each of the plurality of dies (12) is less than the threshold.

Regarding claim 29, Hembree et al disclose repeating measuring [via resistivity measuring circuit 38] the contact resistance and computing [via tester 26] the standard deviation responsive to comparing the standard deviation.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (see PTO-892 for further details).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
September 28, 2005